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# VERIFICATION OF TRANSLATION

I hereby declare and state that I am knowledgeable of each of the German and English languages and that I reviewed the attached translation of the patent application entitled "Carrier Device for Monolithic Integrated Circuits" from the German language into the English language, and that I believe my attached translation to be accurate, true, and correct to the best of my knowledge and ability.

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# Carrier Device for Monolithic Integrated Circuits

This invention relates to a carrier device for a monolithic integrated circuit, the carrier device with the monolithic integrated circuit, the chip, being encapsulated in a thermoplastic material. The plastic encapsulation serves as a package, and the lead fingers coupled to the metallic carrier device, which are connected by bonding wires to the bonding pads of the monolithic integrated circuit, form the package leads. In many circuits it is necessary that the reference potential of the monolithic integrated circuit, usually ground potential or a supply potential, should, if possible, be uniform and undisturbed. To accomplish this in the best possible manner under all operating conditions, most monolithic integrated circuits are connected to the reference potential not only via their backside and the carrier platform, but the circuit itself is connected to the carrier platform via a plurality of additional connections. This is commonly done by providing bonding wires between bonding pads on the chip surface and the carrier platform. To achieve good adhesion of the bonding wires, which are generally gold wires, to the carrier platform of copper, a thin coat of silver, gold, or another suitable material is applied to the carrier platform.

In operation, circuits with high power consumption can reach chip temperatures up to 150 degrees Celsius and more, while in the dead condition, the circuit takes on its ambient temperature, which in automotive applications, for example, may go down to -40 degrees Celsius. As a result, mechanical stresses are produced between the individual materials, because the latter have different coefficients of thermal expansion. This effect increases with the size of the monolithic integrated circuits. For instance, shearing forces occur between the individual layers of the package, of the chip, and of the carrier device. Those shearing forces which occur between the molding compound and the metallization layer of the carrier device are particularly dangerous, because there the adhesive forces are relatively low and the thermal expansion of the metal coating on the carrier platform is very different from the expansion coefficient of the overlying plastic. This affects particularly the bonding pads on the carrier structure. The consequence after many thermal cycles is that the plastic eventually delaminates from the coat surface, so that a relative motion becomes possible. The only mechanical points of fixation are then the bonding pads on the carrier platform, which are overstressed, of course, and finally come off as well, whereby the connection there is severed. As a result, however, the required uniform reference potential can no longer be maintained, so that the performance of the circuit gets increasingly worse until it may eventually fail completely.

It is therefore an object of the invention to remedy this in the least expensive and simplest possible manner.

The object is attained by routing the bonding wires from the chip not directly to the carrier platform, but to raised pedestals connected with the carrier platform. The pedestals rise above the platform plane; because of their relatively steep sides, they form a mechanical point of fixation in the area of the respective bonding pads in relation to lateral motions. The necessary height follows from the plasto-elastic properties of the plastic material and can be optimized by experiment. An appropriate height lies approximately in the range from 1/10 of the chip height to the chip height itself. Or, if the raised pedestal is formed by a drawing or pressing process during the manufacture of the frame using a punchlike tool, the height will range from about 1/10 of the material thickness of the carrier to the carrier thickness itself. These limits follow from the fact that if the raised pedestals are too low, their transition cannot be made steep enough, and if they are too high, the material in the side will become too thin or even rupture. Of course, the steeper the sides are, the better the action of the raised pedestal as a fixed point will be, but this also depends on the properties of the plastic material used. It is even possible to form sides with an angle greater than 90 degrees, for instance by underetching, suitable flanging, or subsequent upsetting. Also important are the transitions at the upper and lower edges of the side, which should, if possible, have only small radii, because otherwise a vertical component,

which would contribute to the detachment of the bonding pads on the raised pedestals, would be added to the shearing component. Thus, the optimum height of the sides and their steepness, which should be at least 45 degrees, are related. For the fixed-point function it is better to have a plurality of raised pedestals on the carrier device, even if not all of the pedestals are used for bonding purposes. The raised pedestals by themselves, i.e. also without bonding pads, are an appropriate measure against other disadvantages of delamination, as a result of which moisture, for example, may penetrate into the package by capillarity.

The raised pedestals form small planes which are parallel to the carrier platform and also allow the formation of more than one bonding pad, for instance pads with a standoff stitch bond. The fact that more than one bonding pad are possible on a raised pedestal does not conflict with the aforementioned requirement for a plurality of pedestals. In many cases, low resistivity can only be achieved by parallel bonding to the respective package lead, and the associated bonding wires should be as short and low-inductance as possible.

If the raised pedestals are located at the edge of the carrier platform, they can be formed by means of a sort of bending-off or folding device, for instance by flanging special carrier regions at the edge of the platform. Another possibility, which need not take the thickness of the carrier material into account, is to form the raised pedestals by application of material, for

instance by soldering on, welding on, or gluing on separate pedestals.

The presence of the raised pedestals also facilitates selective finishing of the carrier device, for instance by silver or gold plating. Because of the shape deviation of the raised pedestals from the remainder of the carrier platform, it is easier to limit the finishing to the pedestals, so that the remainder of the carrier device is left free. Thus, besides a saving of material, better adhesion of the plastic is achieved, as the copper oxide on the carrier surface adheres to the plastic much better than commonly used finishing materials.

A further advantage of the raised pedestals is the reduction of height differences during the bonding of the chip to the lead fingers and the carrier platform.

The invention and further developments thereof will become more apparent from the following description of exemplary embodiments when taken in conjunction with the accompanying drawing, in which:

Fig. 1 shows a cross section of a part of a a raised pedestal;

Fig. 2 is a top view of a multiple-bonded raised pedestal; and

Fig. 3 is a top view of a carrier device with a chip and several raised pedestals.

Fig. 1 is a schematic cross-sectional view of a part of a carrier device 1 with a raised pedestal 2. The section is

taken through the raised pedestal 2, which was formed by means of a punching tool during the manufacture of the frame. In the example shown, the height hp of the pedestal, 120 micrometers, is approximately 1/3 of the carrier height h, which is about 250 micrometers. The optimum of the pedestal height hp lies approximately in a range from 1/5 to twice the material thickness h of the carrier device 1. Compared to the currently common chip height of about 300 micrometers, this corresponds approximately to a range from 1/10 to 1.5 times this chip height. In order to be suitable for multiple bonding, the raised pedestal must have a sufficient length and width, since for each pad diameter, approximately 35 micrometers plus the necessary pad spacing are needed.

Fig. 2 is a top view of a raised pedestal 2 with eight bonding pads 4. The bonding wires 5 and 6 associated with the bonding pads 4 point in different directions. With this raised pedestal 2, two different chips on the carrier platform 1 can thus be connected with the latter by multiple bonding.

Finally, Fig. 3 is a top view of a carrier device 1 providing a platform for a single chip 7, which schematically represents a monolithic integrated circuit. The ten raised pedestals 2 and 2' are located at the edge of the platform, their arrangement being adapted to the requirements of the monolithic integrated circuit. Connections from the chip 7 to the raised pedestals 2 are made by multiple bonding. If the same carrier device 1 is used for different circuits, it is not detrimental if

some of the raised pedestals 2, 2' are not bonded. On the contrary, such unbonded pedestals represent additional points of fixation, which are advantageous within the meaning of the invention. The raised pedestal 2' is one example of an unbonded pedestal. As mentioned, the use of unbonded pedestals 2' is also advantageous where only a remedy against delamination is needed. Of the various bonding connections that can go via the lead fingers 8, 9 or 10 to the signal inputs or outputs of the chip 7 and to the carrier platform 1, only a few examples are shown for illustration.